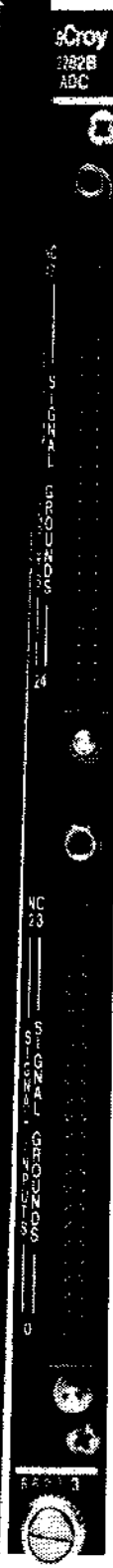
SPECIFICATIONS
CAMAC Model 2282B
48 CHANNEL ADC



Input Sensing:	Charge (current integrating).
Full Scale:	−1000 pC ±10%.
Gain:	−4 counts/pC ±10%
Input Impedance:	50 Ω ±5%; 0 to −50 mA DC.
Input Protection:	±50 V for 1 μsec transients.
Input Limitations:	Maximum voltage for linear response, −1.5 V. For 3 V maximum input linearity is degraded to typically ±(1% of reading +0.25 pC).
Common Mode Properties:	Common Mode Rejection Ratio >50 dB for ±200 mV (DC to 1 kHz).
Integral Linearity:	Typically ±(0.1% of reading of +0.25 pC); worst case ±(0.25% of reading +0.5 pC) for signals of slew rate ≤2 mA/nsec. For signals of slew rate 4 mA/nsec linearity is degraded to typically ±(1% of reading +0.25 pC).
Differential Linearity:	Typically less than 5%.
Residual Pedestal:	Typically 125 counts (subtracted from data by processor) for a gate width of 100 nsec and high source impedance; 250 counts for 500 nsec gate width.
Pedestal-Gate Width Coefficient:	<±50 fC/nsec for gate widths >200 nsec plus 25 fC/nsec if wide gate jumper option is selected.
Temperature Coefficient:	Typically (−0.05% of reading ±0.2 counts)/°C for a gate width of ~1200 nsec. Coefficient may vary slightly for other gate widths.
Long-Term Stability:	±(0.25% of reading +0.5 pC)/week at constant temperature and voltage.
Operating Temperature:	0° to 40°C.
ADC Resolution:	12 bits.
Conversion Time:	1 msec nominal +35 μsec per ADC module.
ADC Isolation:	>60 dB, including the effects of one input connector.
Gate Input:	One per module, rear panel input driven from nonregenerative driver (via ASB) in 2280 System Processor module.
Gate Width:	50 nsec to 5 μsec (10 μsec if wide gate jumper option is implemented). In operation with wide gates, ADC conversion gain depends on pulse position in ADC gate time. This dependence is typically 0.6%/μsec.
Gate Timing:	The gate input to the 2280 System Processor must precede the analog inputs by ≥50 nsec.
Fast Clear:	May be executed any time within 10 μsec of a gate. Settles to within 1 count in <2 μsec.
Digital Clear:	A digital clear is automatically generated by a fast clear ≥10 μsec after the gate; requires 3 μsec to settle.
Test Feature:	Exercised by 2280 System Processor. The charge pulse applied to all channels is proportional to the DC level at the Test Level Input (0 to +10 V). Channel-to-channel matching of the constant of proportionality is <±1%. For 0.0 V Test Level Input each channel's test input is a fixed value within the range 0 to 10 pC. Requires a gate width of ≥1 μsec. For further discussion see Application Note 1.
Analog Outputs:	Current outputs proportional to input (0.5 mA/mA). Risetime >25 nsec, 10-90%. The three output buffers on rear panel are factory wired to sum three groups of 16 channels (0-15, 16-31, 32-47). Gate feedthrough is typically 80 mV (into 50 Ω) for 16 channels, recovered in approximately 120 nsec. Maximum output current for any buffer is 90 mA.
Readout and Control:	Requires one Model 2280/82A Processor per CAMAC crate. LeCroy 2282B's are compatible with 2282A's in the same crate.
Packaging:	No. 1 RF-shielded CAMAC module conforming to ESONE Report EUR 4100 and IEEE Standard 583.
Power Requirement:	770 mA at +6 V 160 mA at +24 V (Plus 1.5 times average input current) 750 mA at −6 V 0 at −24 V
Analog Input Connector:	AMP 102550-1 bulkhead-mounting 25-pair connector. Mates with AMP 2-226651-5 cable connector (AMP-latch series).
Analog Input Cable:	LeCroy Model DK25/50-Length. Includes AMP 2-226298-5 twenty-five lsignal ribbon coaxial cable with termination by AMP 2-226651-5 connectors at both ends (AMP-latch series), plus one AMP 102550-1 one bulkhead-mounting 25-pair connector.

SPECIFICATIONS SUBJECT TO CHANGE